Amendments to the Claims:

The listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A circuit comprising:

a first, second and third voltage divider, each of which comprises resistors having temperature-dependent resistances, outputting a first, second and third voltage; and

a voltage comparator comparing the first voltage with the second voltage, and the first voltage with the third voltage and respectively outputting a first and second signal according to the comparison results.

Claim 2 (currently amended): ~~The circuit as in claim 1, wherein the voltage comparator comprises:~~ A circuit comprising:

a first, second and third voltage divider, each of which comprises resistors having temperature-dependent resistances, outputting a first, second and third divided voltage; and

a voltage comparator comparing the first divided voltage with the second divided voltage, and the second divided voltage with the third divided voltage and respectively outputting a first and second signal according to the comparison results, wherein the voltage comparator comprises:

a first transistor of a first type having a source coupled to receive a first voltage;

a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of a temperature detection signal;

a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;

a fourth transistor of a second type having a drain coupled to a drain of the first transistor and a gate coupled to receive the first divided voltage;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor, a gate coupled to receive the third divided voltage and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor, a gate coupled to receive the second divided voltage and a source coupled to the source of the fourth transistor; and

a seventh transistor of the second type having a drain coupled to the drain of the fourth transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage.

Claim 3 (original): The circuit as in claim 2, wherein the voltage divider comprises:

a first resistor coupled between the gate of the fourth transistor and the source of the first transistor;

a second resistor coupled between the gate of the fourth transistor and the source of the seventh transistor;

a third resistor coupled between the gate of the fifth transistor and the source of the first transistor;

a fourth resistor coupled between the gate of the fifth transistor and the source of the seventh transistor;

a fifth resistor coupled between the gate of the sixth transistor and the source of the first transistor; and

a sixth resistor coupled between the gate of the sixth transistor and the source of the seventh transistor.

Claim 4 (original): The circuit as in claim 2, wherein the first and second types are P and N type, respectively.

Claim 5 (original): The circuit as in claim 2, wherein the first and second voltages are Vdd and a ground voltage, respectively.

Claim 6 (original): The circuit as in claim 3, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

Claim 7 (original). The circuit as in claim 3, wherein the second and third resistors are parasitic resistances of an N well.

Claim 8 (currently amended): ~~The circuit as in claim 1, further comprising:~~ A circuit comprising:

a pulse generating circuit which outputs a periodic pulse train in response to an external control signal;

a frequency-dividing circuit which outputs a plurality of pulse trains having different periods from each other by frequency-dividing said periodic pulse train output by said pulse generating circuit;

a first, second and third voltage divider, each of which comprises resistors having temperature-dependent resistances, outputting a first, second and third divided voltage;

a voltage comparator comparing the first divided voltage with the second divided voltage, and the second divided voltage with the third divided voltage and respectively outputting a first and second signal according to the comparison results;

a voltage detection circuit which detects a power supply voltage applied to said a memory device and outputs a voltage detection signal when said power supply voltage reaches a predetermined voltage level; and

a pulse selection circuit which outputs a self-refresh master clock by selecting one of said pulse trains in response to said first and second signals and said voltage detection signal.

Claim 9 (currently amended). The circuit as in claim ~~8~~18, wherein the first and second type are P and N type, respectively.

Claim 10 (currently amended): The circuit as in claim ~~8~~18, wherein the first and second voltages are Vdd and a ground voltage, respectively.

Claim 11 (currently amended). The circuit as in claim ~~8~~19, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

Claim 12 (currently amended). The circuit as in claim ~~8~~19, wherein the second and third resistors are parasitic resistances of an N well.

Claim 13 (currently amended). ~~The circuit as in claim 1 further comprising:~~ A circuit comprising:

a first, second and third voltage divider, each of which comprises resistors having temperature-dependent resistances, outputting a first, second and third voltage;

a voltage comparator comparing the first voltage with the second voltage, and the first voltage with the third voltage and respectively outputting a first and second signal according to the comparison results;

an internal period selector receiving a plurality of signals representing different periods and outputting one of the signals according to the first and second signals;

a plurality of timers, each generating one of the signals representing the different periods; and

a self-refresh controller determining a refresh period according to the signal output from the internal period selector.

Claim 14 (currently amended). The circuit as in claim ~~13~~20, wherein the first and second type are P and N type, respectively.

Claim 15 (currently amended). The circuit as in claim ~~13~~20, wherein the first and second voltages are Vdd and a ground voltage, respectively.

Claim 16 (currently amended). The circuit as in claim ~~13~~21, wherein the first, fourth, fifth and sixth resistors are made of poly-silicon.

Claim 17 (currently amended). The circuit as in claim ~~13~~21, wherein the second and third resistors are parasitic resistances of an N well.

Claim 18 (new). The circuit as in claim 8, wherein the voltage comparator comprises:

a first transistor of a first type having a source coupled to receive a first voltage;

a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of a temperature detection signal;

a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;

a fourth transistor of a second type having a drain coupled to a drain of the first transistor and a gate coupled to receive the first divided voltage;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor, a gate coupled to receive the third divided voltage and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor, a gate coupled to receive the second divided voltage and a source coupled to the source of the fourth transistor; and

a seventh transistor of the second type having a drain coupled to the drain of the fourth transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage.

Claim 19 (new): The circuit as in claim 18, wherein the voltage divider comprises:

a first resistor coupled between the gate of the fourth transistor and the source of the first transistor;

a second resistor coupled between the gate of the fourth transistor and the source of the seventh transistor;

a third resistor coupled between the gate of the fifth transistor and the source of the first transistor;

a fourth resistor coupled between the gate of the fifth transistor and the source of the seventh transistor;

a fifth resistor coupled between the gate of the sixth transistor and the source of the first transistor; and

a sixth resistor coupled between the gate of the sixth transistor and the source of the seventh transistor.

Claim 20 (new). The circuit as in claim 13, wherein the voltage comparator comprises:

a first transistor of a first type having a source coupled to receive a first voltage;

a second transistor of the first type having a gate coupled to a gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a first bit of a temperature detection signal;

a third transistor of the first type having a gate coupled to the gate of the first transistor, a source coupled to receive the first voltage and a drain outputting a second bit of the temperature detection signal;

a fourth transistor of a second type having a drain coupled to a drain of the first transistor and a gate coupled to receive the first divided voltage;

a fifth transistor of the second type having a drain coupled to the drain of the second transistor, a gate coupled to receive the third divided voltage and a source coupled to a source of the fourth transistor;

a sixth transistor of the second type having a drain coupled to the drain of the third transistor, a gate coupled to receive the second divided voltage and a source coupled to the source of the fourth transistor; and

a seventh transistor of the second type having a drain coupled to the drain of the fourth transistor, a gate coupled to receive an enable signal and a source coupled to receive a second voltage.

Claim 21 (new): The circuit as in claim 20, wherein the voltage divider comprises:

a first resistor coupled between the gate of the fourth transistor and the source of the first transistor;

a second resistor coupled between the gate of the fourth transistor and the source of the seventh transistor;

a third resistor coupled between the gate of the fifth transistor and the source of the first transistor;

a fourth resistor coupled between the gate of the fifth transistor and the source of the seventh transistor;

a fifth resistor coupled between the gate of the sixth transistor and the source of the first transistor; and

a sixth resistor coupled between the gate of the sixth transistor and the source of the seventh transistor.

Claim 22 (new). A circuit comprising:

a first voltage divider comprising a first resistors coupled between a first voltage and a first point and a second resistor coupled between the first point and a second voltage for generating a

first voltage from the first point, wherein a temperature coefficient of the first resistor is smaller than that of the second resistor;

a second voltage divider comprising a third resistor coupled between the first voltage and a second point and a fourth resistor coupled between the second point and the second voltage for generating a second voltage from the second point, wherein a temperature coefficient of the third resistor with that of the fourth resistor are the same

a third voltage divider comprising a fifth resistors coupled between the first voltage and a third point and a sixth resistor coupled between the third point and the second voltage for generating a third voltage from the third point, wherein a temperature coefficient of the sixth resistor is smaller than that of the fifth resistor; and

a voltage comparator comparing the first voltage with the second voltage, and the second voltage with the third voltage and respectively outputting a first and second signal according to the comparison results.

Claim 23 (new). The circuit as in claim 18, wherein the first, third, fourth, and sixth resistors are made of poly-silicon.

Claim 24 (new). The circuit as in claim 18, wherein the second and fifth resistors are parasitic resistances of an N well.